REMARKS

Before considering the several art rejections, it should be noted, as pointed out in the paragraph on the top of page 5 of the subject Application, the present invention provides a device in which a semiconductor chip has at least one chip electrode set comprising at least two chip terminals and bumps for a common wiring layer. This provides redundancy, i.e. so that if the joint at one position becomes separated, the remaining joints are still intact, thereby connection faults are avoided.

Each of the independent claims, namely claims 21-23, 27-29, 33-35 and 39-41 have been amended to stress that the semiconductor chip has at least one chip electrode set comprising at least two chip electrodes in a common wiring layer. This is neither taught nor suggested by the admitted prior art or any of the secondary references.

In rejecting the claims as obvious from the admitted prior art taken with Rostoker and one or more of the secondary references Liang alone, or further in view of Fulcher and optionally further in view of Bertolet et al., the Examiner characterizes Rostoker as teaching three electrodes connected to a common layer in a flip-chip assembly. However, Rostoker's construction does not provide redundancy. Rather, Rostoker employs jumpered contacts as a means for solving routing problems in order to keep signal paths as short as possible. (See column 12, lines 14-17). Applicant's claimed invention, on the other hand, actually sacrifices area occupied by the chip electrodes by providing at least one chip electrode set comprising at least two chip electrodes. In other words, Applicant's claimed invention, contrary to the general trend of reducing area, slightly sacrifices area efficiency to obtain significantly improved reliability. (See the first full paragraph on page 8 of the specification). Accordingly, since neither the admitted prior art, nor any of the secondary references teach or suggest

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semiconductor chip having at least one chip electrode set comprising at least two chip electrodes in a common wiring layer as required by the several independent claims of the subject Application, none of the prior art alone or in any combination reasonably could be said to achieve or render obvious the claimed invention, or the significant advantages thereof as discussed above. Accordingly, the rejections of the claims as obvious from the admitted prior art in view of Rostoker and Liang, or the admitted prior art in view of Rostoker, Liang and Fulcher, or the admitted prior art in view of Rostoker, Liang, Fulcher and Bertolet et al., is in error.

New claims 45-56 have been added to further scope the invention.

Having dealt with all the objections raised by the Examiner, the Application is believed to be in order for allowance.

Pursuant to 37 CFR § 1.121, a marked copy of the amended claims showing changes made therein accompanies this Amendment.

Credit card payment Form PTO-2038 in the amount of $216 accompanies this amendment. In the event there are any fee deficiencies or additional fees are payable, please charge them (or credit any overpayment) to our Deposit Account No. 08-1391.

Respectfully submitted,

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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Assistant Commissioner of Patents, Washington, D.C. 20231 on February 27, 2002, at Manchester, New Hampshire.

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MARKED COPY OF CLAIMS:

21. (Amended) A semiconductor device comprising:

a wiring substrate having a predetermined pattern of wiring formed on one surface;

a semiconductor chip disposed on the other surface of said wiring substrate and having [two or more] at least one chip electrode set comprising at least two chip electrodes in a common wiring layer, wherein said chip electrodes are arranged from an edge of said semiconductor chip toward its inner side;

said wiring substrate having a number of through-holes;

a number of bumps formed respectively in said through-holes in conforming relationship with said [two or more] at least two chip electrodes and electrically connecting said wiring with said [two or more] at least two chip electrodes; and

an external bump pad electrically connected through said common wiring layer to said [two or more] at least two chip electrodes.

22. (Amended) A semiconductor device comprising:

a wiring substrate having a predetermined pattern of wiring formed on one surface;

a semiconductor chip disposed on the other surface of said wiring substrate and having [two or more] at least one chip electrode set comprising at least two chip electrodes in a common wiring layer, wherein said chip electrodes are arranged parallel to an edge of said semiconductor chip and said wiring is bent at at least one position;

said wiring substrate having a number of through-holes;

a number of bumps formed respectively in said through-holes in conforming relationship

with said [two or more] at least two chip electrodes and electrically connecting said wiring with said [two or more] at least two chip electrodes; and

an external bump pad electrically connected through said common wiring layer to said [two or more] at least two chip electrodes.

23. (Amended) A semiconductor device comprising:

a wiring substrate having a predetermined pattern of wiring formed on one surface;

a semiconductor chip disposed on the other surface of said wiring substrate and having [two or more] at least one chip electrode set comprising at least two chip electrodes in a common wiring layer, wherein said chip electrodes are arranged parallel to an edge of said semiconductor chip and said wiring has an end width larger than an inter-electrode distance between said chip electrodes;

said wiring substrate having a number of through-holes;

a number of bumps formed respectively in said through-holes in conforming relationship with said [two or more] at least two chip electrodes and electrically connecting said wiring with said [two or more] at least two chip electrodes; and

an external bump pad electrically connected through said common wiring layer to said [two or more] at least two chip electrodes.

27. (Amended) A semiconductor device comprising:

a wiring substrate having a predetermined pattern of wiring formed on one surface;

a semiconductor chip disposed on said one surface of said wiring substrate and having [two or more] at least one chip electrode set comprising at least two chip electrodes in a common

wiring layer, wherein said chip electrodes are arranged from an edge of said semiconductor chip toward its inner side;

a number of bumps disposed on said wiring respectively in conforming relationship with said [two or more] at least two chip electrodes and electrically connecting said wiring with said [two or more] at least two chip electrodes; and

an external pump pad electrically connected through said common wiring layer to said [two or more] at least two chip electrodes.

28. (Amended) A semiconductor device comprising:

a wiring substrate having a predetermined pattern of working formed on one surface;

a semiconductor chip disposed on said one surface of said wiring substrate and having [two or more] at least one chip electrode set comprising at least two chip electrodes in a common wiring layer, wherein said chip electrodes are arranged parallel to an edge of said semiconductor chip and said wiring is bent at at least one position;

a number of bumps disposed on said wiring respectively in conforming relationship with said [two or more] at least two chip electrodes and electrically connecting said wiring with said [two or more] at least two chip electrodes; and

an external bump pad electrically connected through said common wiring layer to said [two or more] at least two chip electrodes.

29. (Amended) A semiconductor device comprising:

a wiring substrate having a predetermined pattern of wiring formed on one surface;

a semiconductor chip disposed on said one surface of said wiring substrate and having

[two or more] at least one chip electrode set comprising at least two chip electrodes in a common wiring layer, wherein said chip electrodes are arranged parallel to an edge of said semiconductor chip and said wiring has an end width larger than an inter-electrode distance between said chip electrodes;

a number of bumps disposed on said wiring respectively in [confirming] conforming relationship with said [two or more] at least two chip electrodes and electrically connecting said wiring with said [two or more] at least two chip electrodes; and

an external bump pad electrically connected through said common wiring layer to said [two or more] at least two chip electrodes.

33. (Amended) A semiconductor device comprising:

a TAB (tape automated bonding) tape having a predetermined pattern of wiring formed on one surface;

a semiconductor chip disposed on the other surface of said TAB tape and having [two or more] at least one chip electrode set comprising at least two chip electrodes in a common wiring layer, wherein said chip electrodes are arranged from an edge of said semiconductor chip toward its inner side;

said TAB tape having a number of through-holes;

a number of bumps formed respectively in said through-holes in conforming relationship with said [two or more] at least two chip electrodes and electrically connecting said wiring with said [two or more] at least two chip electrodes; and

an external bump pad electrically connected through said common wiring layer to said [two or more] at least two chip electrodes.

34. (Amended) A semiconductor device comprising:

a TAB (tape automated bonding) tape having a predetermined pattern of wiring formed on one surface;

a semiconductor chip disposed on the other surface of said TAB tape and having [two or more] at least one chip electrode set comprising at least two chip electrodes in a common wiring layer, wherein said chip electrodes are arranged parallel to an edge of said semiconductor chip and said wiring is bent at at least one position;

said TAB tape having a number of through-holes;

a number of bumps formed respectively in said through-holes in conforming relationship with said [two or more] at least two chip electrodes and electrically connecting said wiring with said [two or more] at least two chip electrodes; and

an external bump pad electrically connected through said common wiring layer to said [two or more] at least two chip electrodes.

35. (Amended) A semiconductor device comprising:

a TAB (tape automated bonding) tape having a predetermined pattern of wiring formed on one surface;

a semiconductor chip disposed on the other surface of said TAB tape and having [two or more] at least one chip electrode set comprising at least two chip electrodes in a common wiring layer, wherein said chip electrodes are arranged parallel to an edge of said semiconductor chip and said wiring has an end width larger than an inter-electrode distance between said chip electrodes;

said TAB tape having a number of through-holes;

a number of bumps formed respectively in said through-holes in conforming relationship with said [two or more] at least two chip electrodes and electrically connecting said wiring with said [two or more] at least two chip electrodes; and

an external bump pad electrically connected through said common wiring layer to said [two or more] at least two chip electrodes.

39. (Amended) A semiconductor device comprising:

a TAB tape having a predetermined pattern of wiring formed on one surface;

a semiconductor chip disposed on said one surface of said TAB tape and having [two or more] at least one chip electrode set comprising at least two chip electrodes in a common wiring layer, wherein said chip electrodes are arranged from an edge of said semiconductor chip toward its inner side;

a number of bumps disposed on said wiring respectively in conforming relationship with said [two or more] at least two chip electrodes and electrically connecting said wiring with said [two or more] at least two chip electrodes; and

an external bump pad electrically connected through said common wiring layer to said [two or more] at least two chip electrodes.

40. (Amended) A semiconductor device comprising:

a TAB tape having a predetermined pattern of wiring formed on one surface;

a semiconductor chip disposed on said one surface of said TAB tape and having [two or more] at least one chip electrode set comprising at least two chip electrodes in a common wiring layer, wherein said chip electrodes are arranged parallel to an edge of said semiconductor chip

and said wiring is bent at at least one position;

a number of bumps disposed on said wiring respectively in conforming relationship with said [two or more] at least two chip electrodes and electrically connecting said wiring with said [two or more] at least two chip electrodes; and

an external bump pad electrically connected through said common wiring layer to said [two or more] at least two chip electrodes.

41. (Amended) A semiconductor device comprising:

a TAB tape having a predetermined pattern of wiring formed on one surface;

a semiconductor chip disposed on said one surface of said TAB tape and having [two or more] at least one chip electrode set comprising at least two chip electrodes in a common wiring layer, wherein said chip electrodes are arranged parallel to an edge of said semiconductor chip and said wiring has an end width larger than an inter-electrode distance between said chip electrodes;

a number of bumps disposed on said wiring respectively in conforming relationship with said [two or more] at least two chip electrodes and electrically connecting said wiring with said [two or more] at least two chip electrodes; and

an external bump pad electrically connected through said common wiring layer to said [two or more] at least two chip electrodes.